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SERIAL NUMBER	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/229,526	04/19/94	PETERS	M 200730107

EXAMINER	
COURTENAY, J	
ART UNIT	**PAPER NUMBER**
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BAKER & BOTTS
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DATE MAILED: 01/17/96

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

☑ This application has been examined ☑ Responsive to communication filed on 4-19-94 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), 0 days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☑ Notice of References Cited by Examiner, PTO-892.
2. ☑ Notice of Draftsman's Patent Drawing Review, PTO-948.
3. ☑ Notice of Art Cited by Applicant, PTO-1449.
4. ☐ Notice of Informal Patent Application, PTO-152.
5. ☐ Information on How to Effect Drawing Changes, PTO-1474.
6. ☐ _____.

Part II SUMMARY OF ACTION

1. ☑ Claims 1-28 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☑ Claims 1-7, 10-21, 25-28 are rejected.

5. ☑ Claims 8, 9, 22, 23 are objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☑ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on _____. has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____ ; filed on _____.

13. ☐ Since this application apppears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

Response to Patent Application Filing - first office action

This first office action is in response to application **08/229,526** filed in the United States of America on April 19, 1994. **This application is a RULE 47 continuation of U.S. application Ser. No. 08/203/531 (filed Feb. 28, 1994) which is copending.**

JOINT INVENTORS

This application currently names joint inventors. One of the inventors, *David J. Arnold, of 361 Worth Street, Ashboro, NC* [last known address], has elected not to sign the declaration. This Application has been reviewed by the Special Programs Office in response to a petition received Sept. 19, 1994 and was found in compliance with 37 CFR 1.47(a) on Jan. 1, 1995.

As a named inventor Mr. Arnold is entitled to inspect any paper in the file wrapper of this application and may order copies of all or any part thereof (at a prepaid cost per 37 CFR 1.19). Mr. Arnold is entitled to make his position of record in this Application. Alternately, Mr. Arnold may arrange to do any of the preceding through a registered patent attorney or agent upon written authorization being received from Mr. Arnold.

In considering patentability of the claims under 35 U.S.C. § 103, the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. § 1.56 to point out the inventor and

invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. § 102(f) or (g) prior art under 35 U.S.C. § 103.

OBJECTIONS TO THE DRAWINGS

The drawings are objected to because Figures 1 and 2 are not designated by a legend such as "Prior Art". The legend is necessary in order to clarify what applicant's invention is. MPEP § 608.02(g). Correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> *A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*
>
> *Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.*

Claims 1, 4 - 7, 10 - 15, 18 - 21, and 24 - 26 are rejected under 35 U.S.C. § 103 as being unpatentable over Spix et al. (U.S. Patent 5,179,702, issued Jan. 12, 1993) in view of Record et al. (U.S. Patent 5,305,454, issued Apr. 19, 1994, filed Aug. 12, 1991).

As per independent claims 1 and 14:

Spix et al. disclose the invention substantially as claimed, as discussed below:

Spix teaches a method for processing a plurality of processes (i.e., "events") in a processing system having at least one processor. Each discrete process (i.e., "event") is comprised of one or more threads (i.e., a plurality of "segments"). Spix teaches an enhanced software architecture which is an improvement over the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10. This is a symmetrical multiprocessing (SMP) architecture similar to the Sequent Computer system described on page 6 of Applicant's specification [models S2000/450, S2000/750]. Spix teaches that a plurality of segments (i.e., "process queues") are initiated to execute concurrently on at least one processor [col. 9, lines 10 - 15]. Spix teaches that each independent "sub-event" (i.e., "thread") is processed sequentially as determined by priority [col. 9, lines 19 - 23]. It is inherent that the results of the processing are stored. Spix teaches a highly parallel multiprocessor system having multiple tightly-coupled processors that share a common memory which stores "discrete events" (i.e., processes and/or threads).

However, ***Spix*** does not explicitly disclose the processing of a plurality of discrete "events".

Record et al. disclose the processing of a plurality of discrete "events" in the analogous field of endeavor of event handling for the purpose of providing a system which efficiently receives sequential notification of an occurrence of an event [abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the multiprocessor scheduler as taught by **Spix** by implementing the processing of a plurality of discrete "events" [event handling] because it would provide **Spix's** system with the enhanced capability of efficiently receiving sequential notification of an occurrence of an event.

As per claim 4:
Record teaches the monitoring of events (i.e. "segments") [figs. 13, 17]. Record teaches the detection of a failure event [col. 2, lines 63 - 68]. Record teaches the dynamic disabling of an event monitor [col. 2, line 2].

As per claim 5:
Record teaches the dynamic enabling (i.e., re-initializing) and disabling of an event monitor [col. 2, line 2].

As per claim 6:
Record teaches a hierarchy of related event handlers including first (i.e., an "individual event") a second event (i.e., a "master event), and a third event (i.e., a "child event") [abstract].

As per claim 7:
Spix teaches the determination of a number of processors designated for processing [col. 9, lines 30 - 45]. Spix teaches that a user may completely control and tune the performance of multithreaded programs (i.e., a "user override" capability) [col. 12, lines 1 - 5]. Record teaches the determination of the number of events to be processed as a hierarchy of first, second, third, ... nth related event handlers [abstract]. Spix teaches a "segment" or queue of requests to be processed [fig. 4a].

As per claim 10:
Spix teaches a plurality of secondary storage units which store the processing results [fig. 2].

As per claim 11:
Spix teaches an enhanced software architecture which is an improvement over the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10. This is a symmetrical multiprocessing (SMP) architecture similar to the Sequent Computer system described on page 6 of Applicant's specification [models S2000/450, S2000/750].

As per claim 15:
Spix teaches a plurality of processors sharing a single copy of an operating system with each of the processors configured to execute a single process at any one time and each of the processors having read and write access to a least one common memory [abstract, col. 6, lines 7 - 10, col. 7, lines 46 - 59].

As per claim 18:
Record teaches the monitoring of events (i.e. "segments") [figs. 13, 17]. Record teaches the detection of a failure event [col. 2, lines 63 - 68]. Record teaches the dynamic disabling of an event monitor [col. 2, line 2].

As per claim 19:
Record teaches the dynamic enabling (i.e., re-initializing) and disabling of an event monitor [col. 2, line 2].

As per claim 20:
Record teaches a hierarchy of related event handlers including first (i.e., an "individual event") a second event (i.e., a "master event), and a third event (i.e., a "child event") [abstract].

As per claim 21:
Spix teaches the determination of a number of processors designated for processing [col. 9, lines 30 - 45]. Spix teaches that a user may completely control and tune the performance of multithreaded programs (i.e., a "user override" capability) [col. 12, lines 1 - 5]. Record teaches the determination of the number of events to be processed as a hierarchy of first, second, third, ... nth related event handlers [abstract]. Spix teaches a "segment" or queue of requests to be processed [fig. 4a]. Spix teaches work segments that are distributed among the available processors [col. 9, lines 64-65].

As per claim 24:
Spix teaches an enhanced software architecture which is an improvement over the Dynix operating system implemented by Sequent

Computer Systems, as explicitly described in col. 6, lines 7 - 10. This is a symmetrical multiprocessing (SMP) architecture similar to the Sequent Computer system described on page 6 of Applicant's specification [models S2000/450, S2000/750].

As per claims 12, 25:
Spix teaches a parallel processing system [col. 7, line 48].

As per claims 13, 26:
Spix teaches a loosely coupled distributed processing system which uses the Amoeba operating system [col. 5, lines 51, 52].

Claims 2, 3, 16, 17, 27 and 28 are rejected under 35 U.S.C. § 103 as being unpatentable over Spix et al. (U.S. Patent 5,179,702, issued Jan. 12, 1993) in view of Record et al. (U.S. Patent 5,305,454, issued Apr. 19, 1994, filed Aug. 12, 1991), and further in view of Hillis (U.S. Patent 5,303,297, issued Apr. 12, 1994, filed Jul. 25, 1991).

As per claims 2, 3, and 27:
Spix & Record disclose the invention substantially as claimed, as discussed above and further expanded below:

> *Spix teaches a symmetric multiprocessing computer system which uses the Dynix operating system implemented by Sequent Computer Systems, as explicitly described in col. 6, lines 7 - 10. Spix teaches a plurality of processors sharing a single copy of an operating system with each of the processors configured to execute a single process at any one time and each of the processors having read and write access to a least one common*

memory [abstract, col. 6, lines 7 - 10, col. 7, lines 46 - 59]. Spix teaches at least one disk drive which inherently communicates with a system bus through an I/O controller with each of the processors and at least one common memory [fig. 2]. Spix teaches run queue means coupled to the processors for holding a sequential list of "segments" (i.e., jobs or tasks) to be processed [fig. 1b, 4a, 4b]. Spix teaches process creation means and distributing means for distributing the jobs (i.e., "discrete events") [cols. 1, 2, fig. 6b].

However, **Spix & Record** do not explicitly disclose a system for processing customer billing and invoice jobs.

Hillis discloses a system for processing customer billing and invoice jobs in the analogous field of endeavor of real time processing for the purpose of providing a system which efficiently processes large numbers of customer bills and invoices and has the additional feature of delivering the billing information to the subscriber in real time [col. 5, line 39, fig. 2: billing computer 32, abstract].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the multiprocessor scheduler and event handler as taught by **Spix & Record** by implementing a system for processing customer billing because it would provide **Spix & Record's** system with the enhanced capability of efficiently processing large numbers of customer bills and invoices.

As per claim 16:

Hillis discloses a system for processing customer billing which uses a customer account which is tracked in real time, as detailed above in the rejection of claim 14 [abstract, col. 6].

As per claim 17:

Hillis discloses a system for processing a customer account (i.e., "a discrete event") which is tracked in real time, as detailed above in the rejection of claim 14 [abstract, col. 6].

As per claim 28:

Spix teaches that a plurality of segments (i.e., "process queues") are initiated to execute concurrently on at least one processor [col. 9, lines 10 - 15]. Spix teaches that each independent "sub-event" (i.e., "thread") is processed sequentially as determined by priority [col. 9, lines 19 - 23]. It is inherent that the results of the processing are stored. Spix teaches a highly parallel multiprocessor system having multiple tightly-coupled processors that share a common memory which stores "discrete events" (i.e., processes and/or threads).

Prior Art not relied upon:

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent:	**Issued:**	**Inventor:**	**Filed:**
5,359,642	10-25-94	Castro	2-26-93
5,237,684	8-17-93	Record et al.	
5,355,484	10-11-94	Record et al.	8-12-91
5,430,875	7-4-95	Ma	3-31-93

5,062,040	10-29-91	Bishop et al.	9-28-89
5,129,084	7-7-92	Kelly, Jr. et al.	
5,455,952	10-3-95	Gjovaag	11-3-93

Requested Format of Amended Claims:

Please help expedite the prosecution of this application by including the text of all claims which remain in the case in your amendment response. Please label each amended claim as (AMENDED) after the claim number. Please label each unchanged claim (UNCHANGED) after the claim number. Please label each cancelled claim (CANCELLED) after the claim number. The text of a cancelled claim does not need to be included. Please include line numbers in the left margin on each page that contains claims. This format is not mandatory, however, it will help expedite the processing of your application. Your cooperation is appreciated.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **St.John Courtenay III** whose telephone number is **(703) 308-5217.**

Please send all FAX transmissions to **(703) 308-5359.**
Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600.**

ST.JC/ST.JC Dec. 27, 1995

SUPERVISORY PATENT EXAMINER
ART UNIT